IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (currently amended) A tunable ~~Tunable~~ quadrature phase shifter, comprising:

an input means ~~(IN)~~ for inputting an input signal ~~(vin, iin);~~

splitting means ~~(10)~~ for splitting the input signal into two essentially orthogonal first and second signals ~~(i1, i2);~~

adding means ~~(6)~~ for adding said first and second signals ~~(i1, i2);~~

subtracting means ~~(7)~~ for subtracting said first and second signals ~~(i1, i2);~~

a first output ~~(OUT+)~~ for outputting a first output signal ~~(vo1)~~ based on the output signal from said adding means ~~(6);~~ and

a second output ~~(OUT-)~~ for outputting a second output signal ~~(vo2)~~ based on the output signal from said subtracting means ~~(7)~~, ~~characterized in that~~ wherein said splitting means ~~(10)~~ is ~~provided as~~ an all-pass.

2. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 1, ~~characterized by~~ further comprising a first output buffer means ~~(14)~~ for buffering said first output signal ~~(vo1)~~, and a second output buffer means ~~(15)~~ for buffering said second output signal ~~(vo2)~~.

3. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 1, ~~characterized by~~ further comprising a first transimpedance converter ~~(12)~~ having its input connected to said input means ~~(IN)~~.

4. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 1, ~~characterized by~~ further comprising a ~~second~~ first transimpedance converter ~~(14)~~ having its output connected to said first output ~~(OUT+)~~, and a ~~third~~ second transimpedance converter ~~(15)~~ having its output connected to said second output ~~(OUT-)~~.

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5. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 3, ~~characterized in that~~ wherein the transimpedance converter ~~(12; 14; 15)~~ is a transimpedance amplifier.

6. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 2, ~~characterized in that~~ wherein said first and second output buffer means are ~~said second~~ first and ~~third~~ second transimpedance converters ~~(14, 15)~~, respectively.

7. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 1, ~~characterized by~~ comprising at least a first transistor ~~(T.sub.1)~~ with its collector connected to its base and its emitter coupled to a predetermined potential, a second transistor ~~(T.sub.2)~~ with its base connected to the base of said first transistor and its emitter coupled to said predetermined fixed potential, and a capacitor ~~(C)~~ coupled between the junction of the bases of said first and second transistor ~~(T.sub.1, T.sub.2)~~ and said predetermined potential.

8. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 1, ~~provided as a differential phase shifter~~ the splitting means comprising:

a first input ~~(IN+)~~ for inputting an input signal;~~,~~ ~~and~~

a second input ~~(IN-)~~ for inputting an inverse input signal;~~,~~ ~~characterized by at least~~

a first transistor with its collector connected to its base and its emitter coupled to a predetermined potential;~~,~~

a second transistor with its base connected to the base of said first transistor and its emitter coupled to said predetermined potential;~~,~~

a third transistor with its collector connected to its base and its emitter coupled to a predetermined potential;~~,~~

a fourth transistor with its base connected to the base of said third transistor and its collector coupled to said predetermined potential;~~,~~ and

a capacitor ~~(2C)~~ coupled between a first junction of the bases of said first and second transistors and a second junction of the bases of said third and fourth transistors.

9. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 7, ~~characterized in that~~ wherein said transistors are npn transistors.

10. (currently amended) The phase ~~Phase~~ shifter ~~in accordance with~~ of claim 7, ~~characterized in that~~ wherein said predetermined potential is zero ~~(ground)~~.

11. (currently amended) A data ~~Data~~ and clock recovery unit comprising a phase detector ~~(20)~~ which includes a phase shifter ~~in accordance with claim 1~~ having

an input means for inputting an input signal;

splitting means for splitting the input signal into two essentially orthogonal first and second signals;

adding means for adding said first and second signals;

subtracting means for subtracting said first and second signals;

a first output for outputting a first output signal based on the output signal from said adding means; and

a second output for outputting a second output signal based on the output signal from said subtracting means, wherein said splitting means is an all-pass.